EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6004837").PN.	US-PGPUB; USPAT	OR	OFF	2006/03/15 13:46
L2	2779	infineon and (via or trench or opening or hole or groove or aperture) and (semiconductor or amorphous)	US-PGPUB; USPAT	OR	ON	2006/03/15 14:05
L3	31	2 and (crystallization or crystallizing)	US-PGPUB; USPAT	OR	ON	2006/03/15 14:03
L4	22	3 and @ad<"20030923"	US-PGPUB; USPAT	OR	ON	2006/03/15 14:06
L5	481295	(via or trench or opening or hole or groove or aperture) and (semiconductor or amorphous)	US-PGPUB; USPAT	OR	ON	2006/03/15 14:13
L6	9994	5 and ((semiconductor or amorphous) with (crystallization or crystallizing))	US-PGPUB; USPAT	OR	ON	2006/03/15 13:51
L7	7808	6 and @ad<"20030923"	US-PGPUB; USPAT	OR	ON	2006/03/15 14:03
L8	510	7 and trench	US-PGPUB; USPAT	OR	ON	2006/03/15 13:51
L9	256	8 and via	US-PGPUB; USPAT	OR	ON	2006/03/15 14:02
L10	1231	438/269,270,272,589.ccls.	US-PGPUB; USPAT	OR	ON	2006/03/15 14:03
L11	18	10 and (crystallization or crystallizing)	US-PGPUB; USPAT	OR	ON	2006/03/15 14:03
L12	15	11 and @ad<"20030923"	US-PGPUB; USPAT	OR	ON	2006/03/15 14:03
L13	636	((via or trench or opening or hole or groove or aperture) and (semiconductor or amorphous) and (crystallization or crystallizing)).clm.	US-PGPUB; USPAT	OR	ON	2006/03/15 14:06
L14	473	13 and @ad<"20030923"	US-PGPUB; USPAT	OR	ON	2006/03/15 14:06
L15	236904	(via or trench or opening or hole or groove or aperture) and (semiconductor or amorphous)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/15 14:14
L16	739	(via or trench or opening or hole or groove or aperture) and ((crystallization or crystallizing) with (semiconductor or amorphous))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/03/15 14:14

DOCUMENT-IDENTIFIER: US 20040018672 A1

TITLE: Silicon on insulator (SOI) transistor and methods of fabrication

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Claims Text - CLTX (2):
1. A **semiconductor** device comprising: a silicon or silicon alloy film formed on an insulating layer formed on a single crystalline silicon substrate, said silicon film having a single crystalline silicon or silicon alloy portion; a gate dielectric on said single crystalline silicon portion of said silicon film; a gate electrode on said gate dielectric; a source and a drain region formed on opposite sides of said gate electrode in said silicon or silicon alloy film; and a single crystalline silicon or silicon alloy window portion extending from said single crystalline silicon substrate through an **opening** in said insulating layer to said single crystalline silicon or silicon alloy portion of said silicon film.

Claims Text - CLTX (3):
2. The **semiconductor** device of claim 1 wherein said single crystalline silicon or silicon alloy portion of said silicon or silicon alloy film has a thickness of less than 30 nanometers.

Claims Text - CLTX (4):
3. The **semiconductor** device of claim 1 wherein said single crystalline silicon window portion forms part of said source region.

Claims Text - CLTX (5):
4. The **semiconductor** device of claim 1 wherein said silicon or silicon alloy film further includes a polysilicon or an **amorphous** silicon or silicon alloy portion.

Claims Text - CLTX (6):
5. The **semiconductor** device of claim 4 wherein said polysilicon or **amorphous** silicon or silicon alloy portion forms part of said drain region.

Claims Text - CLTX (7):
6. A **semiconductor** device comprising: a silicon or silicon alloy film formed on an insulating layer formed on a single crystalline silicon substrate,

said silicon or silicon alloy film having a single crystalline silicon or silicon alloy portion having a thickness of less than or equal to 30 nanometers; a gate dielectric on said single crystalline silicon or silicon alloy portion of said silicon or silicon alloy film; a gate electrode on said gate dielectric; and a source region and a drain region in said silicon or silicon alloy film on opposite sides of said gate electrode.

Claims Text - CLTX (8):
7. The **semiconductor** device of claim 6 wherein in said silicon or silicon alloy film further comprises an **amorphous** or polycrystalline portion.

Claims Text - CLTX (9):
8. The **semiconductor** device of claim 7 wherein said **amorphous** or polycrystalline portion forms part of said drain region.

Claims Text - CLTX (10):
9. The **semiconductor** device of claim 7 further comprising a single crystalline silicon or silicon alloy window portion extending from said single crystalline silicon substrate through an **opening** in said insulating layer to said single crystalline silicon or silicon alloy portion of said silicon or silicon alloy film.

Claims Text - CLTX (11):
10. The **semiconductor** device of claim 9 wherein said single crystalline silicon or silicon alloy window portion forms part of said source region.

Claims Text - CLTX (12):
11. A **semiconductor** device comprising: a silicon or silicon alloy film formed on an insulating layer formed on a single crystalline silicon substrate, said silicon or silicon alloy film having a single crystalline silicon or silicon alloy portion and an **amorphous** or polycrystalline portion; a gate dielectric on said single crystalline silicon or silicon alloy portion; a gate electrode on said gate dielectric; and a source and a drain region in said silicon or silicon alloy film on opposite sides of said gate electrode.

Claims Text - CLTX (13):
12. The **semiconductor** device of claim 6 further comprising a polish stop layer on said insulating layer adjacent to said silicon film.

Claims Text - CLTX (14):
13. The **semiconductor** device of claim 11 wherein said polish stop layer is selected from the group consisting of silicon nitride and silicon carbide.

Claims Text - CLTX (15):
14. A method of forming a **semiconductor** device comprising: forming an **opening** in an insulating layer formed on a single crystalline silicon substrate; forming an **amorphous** or polycrystalline silicon or silicon alloy layer in said **opening** on said single crystalline silicon substrate and on said insulating layer; and **crystallizing said amorphous** or polycrystalline silicon or silicon alloy film in said **opening** and a least a portion of said **amorphous** or polycrystalline silicon or silicon alloy film formed on said insulating layer into a single crystalline silicon or silicon alloy film.

Claims Text - CLTX (18):
17. The method of claim 14 further comprising forming a dielectric capping layer on said **amorphous** or polycrystalline silicon or silicon alloy film prior to **crystallizing said amorphous** or polycrystalline silicon or silicon alloy film.

Claims Text - CLTX (20):
19. The method of claim 18 wherein said source region includes said single crystalline silicon or silicon alloy film in said **opening**.

Claims Text - CLTX (21):
20. The method of claim 18 wherein said drain region includes a single crystalline silicon or silicon alloy portion and a **amorphous** or polycrystalline silicon or silicon alloy portion.

Claims Text - CLTX (22):
21. The method of claim 14 wherein said **amorphous** or polycrystalline silicon or silicon alloy film is formed to a thickness less than 30 nanometers.

Claims Text - CLTX (23):
22. The method of claim 14 wherein said **crystallization** step comprises a laser anneal.

Claims Text - CLTX (24):
23. The method of claim 14 wherein said **crystallization** step includes a high temperature anneal.

Claims Text - CLTX (25):
24. A method of forming a **semiconductor** device comprising: forming a polish stop layer on a insulating layer formed on a single crystalline silicon substrate; forming an **opening** in said polish stop layer; forming an **opening**

in said insulating layer within said **opening** in said polish stop layer; forming an **amorphous** or polycrystalline silicon or silicon alloy film in said **opening** on said single crystalline silicon substrate in said **opening** of said insulating layer, on said insulating layer within said **opening** in said polish stop layer, and on said polish stop layer; **crystallizing said amorphous** or polycrystalline silicon or silicon alloy film in said **opening** in said insulating layer and at least a portion of said **amorphous** or polycrystalline silicon or silicon alloy film formed on said insulating layer within said polish stop layer into a single crystalline silicon or silicon alloy film; and polishing said single crystalline silicon or silicon alloy film on said insulating layer until said single crystalline silicon or silicon alloy film is removed from said polish stop layer and is substantially planar with said polish stop layer.

Claims Text - CLTX (28):
27. The method of claim 24 further comprising forming a dielectric capping layer on said **amorphous** or polycrystalline silicon or silicon alloy film prior to **crystallizing said amorphous** or polycrystalline silicon or silicon alloy film.

Claims Text - CLTX (30):
29. The method of claim 28 wherein said source region includes said single crystalline silicon or silicon alloy film in said **opening**.

Claims Text - CLTX (31):
30. The method of claim 28 wherein said drain region includes a single crystalline silicon or silicon alloy portion and a **amorphous** or polycrystalline silicon or silicon alloy portion.

Claims Text - CLTX (32):
31. The method of claim 24 wherein said **amorphous** or polycrystalline silicon or silicon alloy film is formed to a thickness greater than >100 nanometers.

Claims Text - CLTX (33):
32. The method of claim 24 wherein said **crystallization** step comprises a laser anneal.

Claims Text - CLTX (34):
33. The method of claim 24 wherein said **crystallization** step includes a high temperature anneal.